CLAIMS

What is claimed is:

1. A processor, comprising:

an overflow/underflow control bit;

a programmable saturation control bit;

a processing unit that produces an unsaturated output;

a saturation unit coupled to the processing unit and that produces an output that is saturated when the overflow/underflow control bit is set indicating the occurrence of an underflow or overflow condition; and

a selection unit that receives the outputs from the processing and saturation units and selects one of the two outputs as an output from the selection unit based on the state of the saturation control bit.

2. The processor of claim 1 wherein the processing unit comprises an arithmetic logic unit.

3. The processor of claim 1 wherein the processing unit comprises a multiply and accumulate unit.

4. The processor of claim 1 wherein the selection unit comprises a multiplexer.

5. The processor of claim 1 wherein the saturation unit forces the saturated output to be a maximum value if an overflow occurs in the processing unit.

6. The processor of claim 1 wherein the saturation unit forces the saturated output to be a minimum value if an underflow occurs in the processing unit.

7. The processor of claim 1 wherein the saturation control bit is programmed through an application programming interface.

8. The processor of claim 1 wherein the saturation control bit is programmed through an assembly language macro that is instantiated in high-level code.

9. The processor of claim 1 wherein the saturation control bit is programmed through a compiler through a specific pragma.

10. The processor of claim 1 wherein the saturation control remains set for multiple instructions.

11. A method for performing saturated arithmetic, comprising:

receiving an unsaturated output from a processing unit;

processing the unsaturated output to produce a saturated output based upon the state of an overflow/underflow control bit that indicates whether an overflow or underflow condition has occurred; and

selecting between the saturated output and unsaturated output based on the state of a programmable saturation control bit.

12. The method of claim 11 wherein the saturation control bit is programmed through an application programming interface to cause either saturated or non-saturated operations to be performed.

13. The method of claim 11 wherein processing the unsaturated output comprises forcing the saturated output to be a maximum value if an overflow occurs in the processing unit.

14. The method of claim 11 wherein processing the unsaturated output comprises forcing the saturated output to be a minimum value if an underflow occurs in the processing unit.

15. A processor, comprising:

a means for performing an unsaturated operation to produce an unsaturated value;

a means for saturating the unsaturated value to produce a saturated value;

a means for dynamically selecting between the unsaturated value and the saturated value based upon a mode bit that indicates whether saturated or unsaturated operations are to be performed.

16. The processor of claim 15 further comprising a means for setting the mode bit.

17. The processor of claim 15 wherein the mode bit remains set for the execution of multiple instructions.